PVP 20

Code: 20EC3603

III B.Tech - II Semester – Regular Examinations – JUNE 2023

VLSI DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	Describe a Verilog module for full subtractor using structural modeling.	L2	CO1	7 M
	b)	Describe Verilog module for 4 to 1 Mux using gate level modeling.	L2	CO1	7 M
OR					
2	a)	Discuss a Verilog code for 2 to 4 decoder using data flow modeling.	L2	CO1	7 M
	b)	Discuss a Verilog code for half adder using gate level modeling.	L2	CO1	7 M
UNIT-II					
3	a)	Realize a boolean functions $F1(A, B, C) = \sum m(1, 2, 5, 7)$ and $F2(A, B, C) = \sum m(0, 3, 4, 6)$ using PAL.	L3	CO2	7 M
	b)	Demonstrate the different types of FPGA architecture with neat diagram.	L3	CO2	7 M

		OR			
4	a)	How to realize the Boolean expression X = AB + AB'C' + BC' and Y = BC + A'BC' + ABC using PAL.	L3	CO2	7 M
	b)	Distinguish FPGA and CPLD.	L3	CO2	7 M
		UNIT-III			
5	a)	Explain the fabrication steps involved in NMOS transistor with neat sketches.	L4	CO3	7 M
	b)	Compare CMOS and BICMOS Technologies.	L4	CO3	7 M
		OR			
6	a)	Analyze characteristics of enhancement mode nMOS transistor.	L4	CO3	7 M
	b)	Compare NMOS and GaAs Technologies.	L4	CO3	7 M
		UNIT-IV			
7	a)	Derive the Drain current equation for three regions of nMOS transistor and draw its V-I characteristics.	L4	CO3	7 M
	b)	Analyze the stick diagram for 3 input NOR gate.	L4	CO3	7 M
		OR			
8	a)	Derive the required ratio between Zp.u. and Zp.d. if an nMOS inverter is to be driven from another nMOS inverter.	L4	CO3	7 M
	b)	Analyze the stick diagram for the following function Y = (A+B)C	L4	CO3	7 M

UNIT-V					
9	a)	Explain the various factors involved in limits of scaling of devices.	L4	CO4	7 M
	b)	Realize a 2:1 MUX using Pass Transistor logic.	L3	CO4	7 M
OR					
10	a)	Explain the scaling factors involved in Full Scaling method in VLSI.	L4	CO4	7 M
	b)	Realize a 2:1 MUX using Transmission gate logic.	L3	CO4	7 M